SYSTEM AND METHOD FOR SIMULATION OF AN INTEGRATED CIRCUIT DESIGN USING A HIERARCHICAL INPUT NETLIST AND DIVISIONS ALONG HIERARCHICAL BOUNDARIES THEREOF

ABSTRACT OF THE DISCLOSURE

A system and a method for performing circuit simulation on a integrated circuit design that is represented by a hierarchical netlist. The system and method utilize, in one embodiment, an event driven simulator that divides or "cuts" along the hierarchical boundaries of the input netlist in order to produce subcircuits that are then converted into their Thevenin equivalents. Once a Thevenin equivalent is computed, matrix computations are used to compute the cut node voltages and sensitivity vectors may be used to then determine the internal node voltages. This is done for each event. In the event driven example, a group of leaf cells are identified that are touched by a given event. This group is then cut based on the hierarchical boundaries of the input netlist. The system maintains dynamic node voltages across the entire netlist and also maintains instance specific dynamic information for each cell. However, static information for a given cell is shared for each cell instance thereby reducing memory resources required to perform simulation for input hierarchical netlists that contain repeated cell instances. The present invention provides an accurate voltage and current simulation while requiring reduced memory resources for hierarchical netlists that contain repeated cell instances.